RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, DECEMBER 2016

FIRST YEAR [BATCH 2016-19]

Date : 15/12/2016 **COMPUTER SCIENCE [General]**

Time : 11 am – 1 pm **Paper : I** Full Marks : 50

[Use a separate Answer Book for each Group]

Group – A

Answer <u>any one</u> question : [1×5]

1. a) Find the complement of the function : $f(x, y, z) = xyz' + x'yz + xy'z'$. [2]
   b) Find the Gray code for the binary code $(111001)_2$. [3]
2. a) Perform the following conversion : $(101101 \cdot 1101)_2 = (?)_8$. [3]
   b) What is the 2's complement of $(1010101)_2$? [2]

Answer <u>any two</u> questions : [2×10]

3. a) Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum. [3]
   b) Using 1's complement method, subtract $(11011)_2$ from $(1001)_2$. [2]
   c) Determine the base of the number for the following operation to be correct : 24 + 17 = 40 [2]
   d) Write a short note on Hamming code. [3]
4. a) Draw the circuit diagram for 3-bit even parity generator. [2]
   b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals $(BC' + A'D)(AB' + CD')$. [3]
   c) Write De Morgan's Laws. [2]
   d) Using XOR gate, design an inverter. [3]
5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code. [5]
   b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. $F(A, B, C, D) = \sum(1, 3, 5, 7, 9, 15)$; $d(A, B, C, D) = \sum(4, 6, 12, 13)$. [5]
6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from $f(A, B, C) = ABC + AB'C' + AB'C + ABC' + A'B'C$. [6]
   b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred. [4]

Group – B

Answer <u>any one</u> question : [1×5]

7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2·5]
8. What is a zero address instruction? Write down the program to evaluate $X = (A + B) * (C + D)$ for a stack-organized computer and identify the zero address instructions. [1+3+1]

Answer <u>any two</u> questions : [2×10]

9. a) Design a 2-bit comparator circuit with necessary logic gates. [4]
   b) How does a master-slave flop-flop avoid the race-around condition? [3]
   c) Convert a D flip-flop into a T flipflop. [3]

10. a) 'A 3-to-8 decoder with an Enable input is a 1-to-8-demultiplexer' —Explain. [3]

b) Implement the following logic function using 8 : 1 multiplexer.

$F(A, B, C, D) = \sum m(1, 2, 5, 6, 7, 8, 10, 12, 13, 15)$. [3]

c) What is the role of the cache memory in the memory hierarchy? [2]

d) Differentiate between SRAM and DRAM. [2]

11. a) Design a synchronous counter which will count the following states 0, 3, 5, 6, 0, ... [Use negative edge triggered T flip flop] [5]

b) Explain program-controlled I/O method. [3]

c) What is meant by the register addressing mode? [2]

12. a) Realise a J-K flip flop using a S-R flip flop. [4]

b) What are the basic components of the Von Neumann architecture. [2]

c) Design a full subtractor. Also write down its working principle. [2+2]

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