## **RAMAKRISHNA MISSION VIDYAMANDIRA**

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, DECEMBER 2016

FIRST YEAR [BATCH 2016-19]

COMPUTER SCIENCE [General]

Date : 15/12/2016 Time : 11 am - 1 pm

Answer any one question :

## Paper : I

Full Marks : 50

## [Use a separate Answer Book for each Group]

## $\underline{Group-A}$

<ul> <li>b) Find the Gray code for the binary code (111001)<sub>2</sub>.</li> <li>a) Perform the following conversion : (101101·1101)<sub>2</sub> = (?)<sub>8</sub>.</li> <li>b) What is the 2's complement of (1010101)<sub>2</sub>?</li> <li>Answer any two questions : [2×1]</li> <li>3. a) Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum. [10]</li> <li>b) Using 1's complement method, subtract (11011)<sub>2</sub> from (1001)<sub>2</sub>. [2]</li> <li>c) Determine the base of the number for the following operation to be correct : 24 + 17 = 40 [2]</li> <li>d) Write a short note on Hamming code. [2]</li> <li>4. a) Draw the circuit diagram for 3-bit even parity generator. [3]</li> <li>b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of litertals (BC' + AD)(AB' + CD').</li> <li>c) Write De Morgan's Laws. [3]</li> <li>d) Using XOR gate, design an inverter. [3]</li> <li>a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code. [4]</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1, 3, 5, 7, 9, 15); d(A, B, C, D) = ∑(4, 6, 12, 13). [4]</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C + AB'C + AB'C + AB'C + AB'C + [4]</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred. [4]</li> <li>7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2-5+2-2]</li> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+4]</li> <li>Answer any two questions : [1+3+4]</li> <li>Answer any two questions : [2+5+2]</li> <li>8. What is a zero address instruct</li></ul>	1.	a)	Find the complement of the function : $f(x, y, z) = xyz' + x'yz + xy'z'$ .	[2]				
<ul> <li>2. a) Perform the following conversion : (101101·1101)<sub>2</sub> = (?)<sub>8</sub>. []</li> <li>b) What is the 2's complement of (1010101)<sub>2</sub>?</li> <li>Answer any two questions : [2×1]</li> <li>3. a) Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum. []</li> <li>b) Using 1's complement method, subtract (11011)<sub>2</sub> from (1001)<sub>2</sub>. []</li> <li>c) Determine the base of the number for the following operation to be correct : 24 + 17 = 40 []</li> <li>d) Write a short note on Hamming code. []</li> <li>4. a) Draw the circuit diagram for 3-bit even parity generator. []</li> <li>b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals (BC' + AD)(AB' + CD'). []</li> <li>c) Write De Morgan's Laws. []</li> <li>d) Using XOR gate, design an inverter. []</li> <li>5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code. []</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1, 3, 5, 7, 9, 15); d(A, B, C, D) = ∑(4, 6, 12, 13). []</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + ABC' + A'B'C. []</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred. []</li> <li>7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. []</li> <li>7. Design a 2-bit comparator circuit with necessary logic gates. []</li> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instruction? []</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates. []</li> <li>b) How does a master-slave flop-flop avoid the race-arou</li></ul>		b)	Find the Gray code for the binary code $(111001)_2$ .	[3]				
b) What is the 2's complement of $(1010101)_2$ ? Answer <u>any two</u> questions : [2×1] 3. a) Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum. [2×1] b) Using 1's complement method, subtract $(11011)_2$ from $(1001)_2$ . [2] c) Determine the base of the number for the following operation to be correct : $24 + 17 = 40$ [2] d) Write a short note on Hamming code. [2] 4. a) Draw the circuit diagram for 3-bit even parity generator. [2] b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals (BC' + A'D)(AB' + CD'). [2] c) Write De Morgan's Laws. [2] d) Using XOR gate, design an inverter. [2] 5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code. [3] b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = $\sum (1, 3, 5, 7, 9, 15)$ ; $d(A, B, C, D) = \sum (4, 6, 12, 13)$ . [3] 6. a) Convert the following sone-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + AB'C + ABC' + A'B'C. [4] b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is $0 \ 0 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0$	2.	a)	Perform the following conversion : $(101101 \cdot 1101)_2 = (?)_8$ .	[3]				
Answer <u>any two</u> questions:       [2×1]         3. a) Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum.       []         b) Using 1's complement method, subtract (11011) <sub>2</sub> from (1001) <sub>2</sub> .       []         c) Determine the base of the number for the following operation to be correct: $24 + 17 = 40$ []         d) Write a short note on Hamming code.       []         4. a) Draw the circuit diagram for 3-bit even parity generator.       []         b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals (BC' + A'D)(AB' + CD').       []         c) Write De Morgan's Laws.       []         d) Using XOR gate, design an inverter.       []         5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code.       []         b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = $\sum (1, 3, 5, 7, 9, 15); d(A, B, C, D) = \sum (4, 6, 12, 13).$ []         6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from $f(A, B, C) = ABC + ABC' + ABC' + ABC' + A'BC'.$ []         b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is $0 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ $		b)	What is the 2's complement of (1010101) <sub>2</sub> ?	[2]				
<ul> <li>3. a) Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum.</li> <li>b) Using 1's complement method, subtract (11011)<sub>2</sub> from (1001)<sub>2</sub>.</li> <li>c) Determine the base of the number for the following operation to be correct : 24 + 17 = 40</li> <li>d) Write a short note on Hamming code.</li> <li>4. a) Draw the circuit diagram for 3-bit even parity generator.</li> <li>b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals (BC' + A'D)(AB' + CD').</li> <li>c) Write De Morgan's Laws.</li> <li>d) Using XOR gate, design an inverter.</li> <li>3. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code.</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1,3,5,7,9,15); d(A, B, C, D) = ∑(4,6,12,13).</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + AB'C + AB'C + AB'C + AB'C + C = ABC' + AB'C +</li></ul>	An	Answer <u>any two</u> questions : [2×10]						
<ul> <li>c) Defermine the base of the number for the following operation to be correct : 24 + 17 = 40</li> <li>d) Write a short note on Hamming code.</li> <li>4. a) Draw the circuit diagram for 3-bit even parity generator.</li> <li>b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals (BC' + A'D)(AB' + CD').</li> <li>c) Write De Morgan's Laws.</li> <li>d) Using XOR gate, design an inverter.</li> <li>5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code.</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1, 3, 5, 7, 9, 15); d(A, B, C, D) = ∑(4, 6, 12, 13).</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + AB'C + AB'C'.</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 0. Consider only single bit error may be occurred.</li> <li><b>Caroup – B</b></li> <li>Answer any one question : <ul> <li>[1&gt;x</li> <li>[1&gt;x</li> <li>[1&gt;x</li> </ul> </li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates.</li> <li>b) How does a master-slave flop-flop avoid the race-around condition?</li> <li>c) Convert a D flip-flop into a T flipflop.</li> </ul>	3.	a) b)	Represent the unsigned decimal numbers 965 and 672 in BCD and then show the steps necessary to form their sum. Using 1's complement method, subtract (11011) <sub>2</sub> from (1001) <sub>2</sub>	[3]				
<ul> <li>4. a) Draw the circuit diagram for 3-bit even parity generator.</li> <li>b) Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals (BC' + A'D)(AB' + CD').</li> <li>c) Write De Morgan's Laws.</li> <li>d) Using XOR gate, design an inverter.</li> <li>5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code.</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1,3,5,7,9,15); d(A, B, C, D) = ∑(4,6,12,13).</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + AB'C + AB'C.</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred.</li> <li>Coroup - B</li> <li>Answer any one question : [1×7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2·2</li> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer any two questions : [2×1]</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates.</li> <li>b) How does a master-slave flop-flop avoid the race-around condition?</li> <li>c) Convert a D flip-flop into a T flipflop.</li> </ul>		c) d)	Determine the base of the number for the following operation to be correct : $24 + 17 = 40$ Write a short note on Hamming code.	[2] [2] [3]				
<ul> <li>c) Write De Morgan's Laws.</li> <li>d) Using XOR gate, design an inverter.</li> <li>5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code.</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1,3,5,7,9,15); d(A, B, C, D) = ∑(4,6,12,13).</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C + AB'C + ABC' + A'B'C.</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred.</li> <li>Caroup – B</li> <li>Answer any one question : [1×7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2-5+2-2:8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer any two questions : [2×1]</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates.</li> <li>b) How does a master-slave flop-flop avoid the race-around condition?</li> <li>c) Convert a D flip-flop into a T flipflop.</li> </ul>	4.	a) b)	Draw the circuit diagram for 3-bit even parity generator. Using Boolean algebra, simplify the following Boolean expression to a minimum number of literals $(BC' + A'D)(AB' + CD')$ .	[2] [3]				
<ul> <li>5. a) Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code.</li> <li>b) Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. F(A, B, C, D) = ∑(1,3,5,7,9,15); d(A, B, C, D) = ∑(4,6,12,13).</li> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + AB'C + ABC' + A'B'C.</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred.</li> <li>Caroup – B</li> <li>Answer any one question : [1×7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2·8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer any two questions : [2×1]</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates.</li> <li>b) How does a master-slave flop-flop avoid the race-around condition?</li> <li>c) Convert a D flip-flop into a T flipflop.</li> </ul>		c) d)	Write De Morgan's Laws. Using XOR gate, design an inverter.	[2] [3]				
<ul> <li>6. a) Convert the following sum-of-product expression to its equivalent product-of-sum from f(A, B, C) = ABC + AB'C' + AB'C + A'B'C .</li> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred.</li> <li><i>Group – B</i></li> <li><i>Answer any one question</i> : [1&gt;</li> <li>7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2-8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li><i>Answer any two questions</i> : [2×19. a) Design a 2-bit comparator circuit with necessary logic gates. b) How does a master-slave flop-flop avoid the race-around condition? [1]</li> </ul>	5.	a) b)	Design a circuit to convert a 3-bit Gray Code to its equivalent Excess-3 code. Simplify the following Boolean function F, together with the don't care condition d, into sum of minterms. $F(A, B, C, D) = \sum (1, 3, 5, 7, 9, 15)$ ; $d(A, B, C, D) = \sum (4, 6, 12, 13)$ .	[5] [5]				
<ul> <li>b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 0 0 0 1 1 0 0 1 0 1 0 0. Consider only single bit error may be occurred.</li> <li><u>Group – B</u></li> <li>Answer any one question : [1&gt;</li> <li>7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2-3.</li> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer any two questions : [2×1</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates.</li> <li>b) How does a master-slave flop-flop avoid the race-around condition?</li> <li>c) Convert a D flip-flop into a T flipflop.</li> </ul>	6.	a)	Convert the following sum-of-product expression to its equivalent product-of-sum from $f(A, B, C) = ABC + AB'C' + AB'C + ABC' + A'B'C$ .	[6]				
Group – B       [1×         Answer any one question :       [1×         7. Design a 3-bit Universal Shift Register (USR) by explaining its operation.       [2·5+2·4]         8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions.       [1+3+         Answer any two questions :       [2×1]         9. a) Design a 2-bit comparator circuit with necessary logic gates.       [         b) How does a master-slave flop-flop avoid the race-around condition?       [         c) Convert a D flip-flop into a T flipflop.       [		b)	A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is $000110010100$ . Consider only single bit error may be occurred.	[4]				
<ul> <li>Answer <u>any one question</u>: [1&gt;</li> <li>7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2-</li> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer <u>any two questions</u>: [2×1</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates. [2×1</li> <li>b) How does a master-slave flop-flop avoid the race-around condition? [2&lt;00, 100, 100, 100, 100, 100, 100, 100,</li></ul>	<u>Group – B</u>							
<ul> <li>7. Design a 3-bit Universal Shift Register (USR) by explaining its operation. [2·5+2</li> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer any two questions : [2×1</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates. [</li> <li>b) How does a master-slave flop-flop avoid the race-around condition? [</li> <li>c) Convert a D flip-flop into a T flipflop. [</li> </ul>	An	swer	any one question :	[1×5]				
<ul> <li>8. What is a zero address instruction? Write down the program to evaluate X = (A+B)*(C+D) for a stack-organized computer and identify the zero address instructions. [1+3+</li> <li>Answer any two questions : [2×1]</li> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates. [</li> <li>b) How does a master-slave flop-flop avoid the race-around condition? [</li> <li>c) Convert a D flip-flop into a T flipflop. [</li> </ul>	7.	Des	sign a 3-bit Universal Shift Register (USR) by explaining its operation. [2.5-	+2.5]				
Answer any two questions :       [2×1]         9. a) Design a 2-bit comparator circuit with necessary logic gates.       [         b) How does a master-slave flop-flop avoid the race-around condition?       [         c) Convert a D flip-flop into a T flipflop.       [	8.	Wh stac	What is a zero address instruction? Write down the program to evaluate $X = (A+B)*(C+D)$ for a stack-organized computer and identify the zero address instructions. [1+3+1]					
<ul> <li>9. a) Design a 2-bit comparator circuit with necessary logic gates.</li> <li>b) How does a master-slave flop-flop avoid the race-around condition?</li> <li>c) Convert a D flip-flop into a T flipflop.</li> </ul>	An	swer	<u>any two</u> questions : [2	2×10]				
	9.	a) b) c)	Design a 2-bit comparator circuit with necessary logic gates. How does a master-slave flop-flop avoid the race-around condition? Convert a D flip-flop into a T flipflop.	[4] [3] [3]				

10.	a)	'A 3-to-8 decoder with an Enable input is a 1-to-8-demultiplexer' — Explain.	[3]
	b)	Implement the following logic function using 8 : 1 multiplexer.	
		$F(A, B, C, D) = \sum m(1, 2, 5, 6, 7, 8, 10, 12, 13, 15).$	[3]
	c)	What is the role of the cache memory in the memory hierarchy?	[2]
	d)	Differentiate between SRAM and DRAM.	[2]
11.	a)	Design a synchronous counter which will count the following states 0, 3, 5, 6, 0, [Use negative edge triggered T flip flop]	e [5]
	b)	Explain program-controlled I/O method.	[3]
	c)	What is meant by the register addressing mode?	[2]
12.	a)	Realise a J-K flip flop using a S-R flip flop.	[4]
	b)	What are the basic components of the Von Neumann architecture.	[2]
	c)	Design a full subtractor. Also write down its working principle.	[2+2]

\_\_\_\_\_ × \_\_\_\_\_